

74VCXH16240

Low-Voltage 1.8/2.5/3.3V 16-Bit Buffer

With 3.6 V –Tolerant Inputs and Outputs (3–State, Inverting)

The 74VCXH16240 is an advanced performance, inverting 16–bit buffer. It is designed for very high–speed, very low–power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be overvoltage tolerant to 3.6 V.

The 74VCXH16240 is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16–bit operation. The 3–state outputs are controlled by an Output Enable ($\overline{OE_n}$) input for each nibble. When $\overline{OE_n}$ is LOW, the outputs are on. When $\overline{OE_n}$ is HIGH, the outputs are in the high impedance state. The data inputs include active bushold circuitry, eliminating the need for external pullup resistors to hold unused or floating inputs at a valid logic state.

Features

- Designed for Low Voltage Operation: $V_{CC} = 1.65\text{ V} - 3.6\text{ V}$
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 2.5 ns max for 3.0 V to 3.6 V
3.0 ns max for 2.3 V to 2.7 V
6.0 ns max for 1.65 V to 1.95 V
- Static Drive: $\pm 24\text{ mA}$ Drive at 3.0 V
 $\pm 18\text{ mA}$ Drive at 2.3 V
 $\pm 6\text{ mA}$ Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- Includes Active Bushold to Hold Unused or Floating Inputs at a Valid Logic State
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0\text{ V}^*$
- Near Zero Static Supply Current in All Three Logic States (20 μA)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds $\pm 250\text{ mA}$ @ 125°C
- ESD Performance: Human Body Model >2000 V
Machine Model >200 V
- All Devices in Package TSSOP are Inherently Pb–Free**

*To ensure the outputs activate in the 3–state condition, the output enable pins should be connected to V_{CC} through a pullup resistor. The value of the resistor is determined by the current sinking capability of the output connected to the \overline{OE} pin.

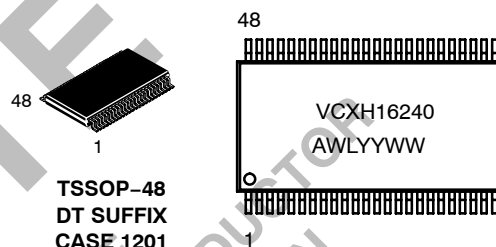
**For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



TSSOP–48
DT SUFFIX
CASE 1201

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
74VCXH16240DT	TSSOP (Pb–Free)	39 / Rail
74VCXH16240DTR	TSSOP (Pb–Free)	2500 / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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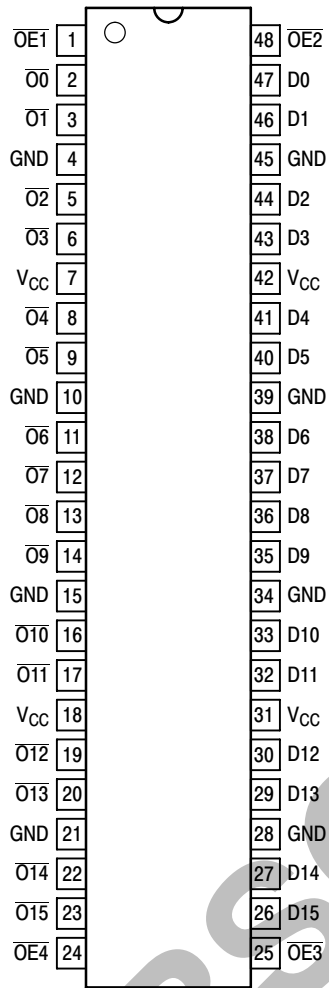


Figure 1. 48-Lead Pinout
(Top View)

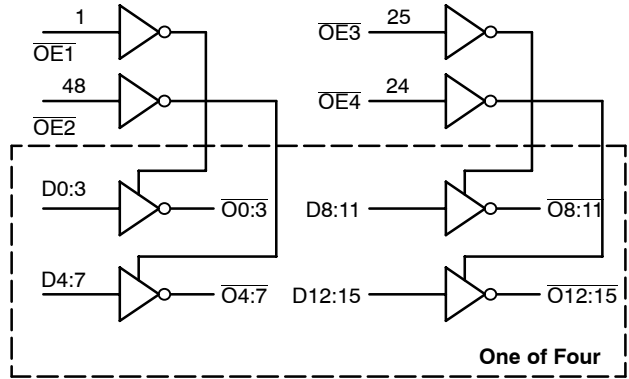


Figure 2. Logic Diagram

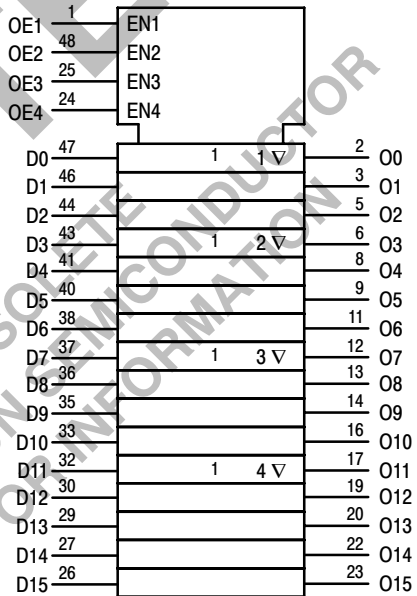


Figure 3. IEC Logic Diagram

Table 1. PIN NAMES

Pins	Function
OE _n D0–D15 O0–O15	Output Enable Inputs Inputs Outputs

TRUTH TABLE

OE1	D0:3	O0:3	OE2	D4:7	O4:7	OE3	D8:11	O8:11	OE4	D12:15	O12:15
L	L	H	L	L	H	L	L	H	L	L	H
L	H	L	L	H	L	L	H	L	L	H	L
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level

L = Low Voltage Level

Z = High Impedance State

X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +4.6		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +4.6		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ +4.6	Output in 3-State	V
		-0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1; Outputs Active	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	Operating	1.65	3.3	3.6	V
		Data Retention Only	1.2	3.3	3.6	
V _I	Input Voltage	-0.3		3.6	V	
V _O	Output Voltage	(Active State)	0		V _{CC}	V
		(3-State)	0		3.6	
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0 V – 3.6 V			-24	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 3.0 V – 3.6 V			24	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 2.3 V – 2.7 V			-18	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 2.3 V – 2.7 V			18	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 1.65 V – 1.95 V			-6	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 1.65 V – 1.95 V			6	mA	
T _A	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V	

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V	0.65 × V _{CC}		V
		2.3 V ≤ V _{CC} ≤ 2.7 V	1.6		
		2.7 V < V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V		0.35 × V _{CC}	V
		2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	
		2.7 V < V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2		V
		V _{CC} = 1.65 V; I _{OH} = -6 mA	1.25		
		V _{CC} = 2.3 V; I _{OH} = -6 mA	2.0		
		V _{CC} = 2.3 V; I _{OH} = -12 mA	1.8		
		V _{CC} = 2.3 V; I _{OH} = -18 mA	1.7		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 1.65 V; I _{OL} = 6 mA		0.3	
		V _{CC} = 2.3 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 2.3 V; I _{OL} = 18 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 18 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _I	Input Leakage Current	1.65 V ≤ V _{CC} ≤ 3.6 V; 0V ≤ V _I ≤ 3.6 V		±5.0	μA
I _{I(HOLD)}	Minimum Bushold Input Current	V _{CC} = 3.0 V, V _{IN} = 0.8 V	75		μA
		V _{CC} = 3.0 V, V _{IN} = 2.0 V	-75		
		V _{CC} = 2.3 V, V _{IN} = 0.7 V	45		
		V _{CC} = 2.3 V, V _{IN} = 1.6 V	-45		
		V _{CC} = 1.65 V, V _{IN} = 0.57 V	25		
		V _{CC} = 1.65 V, V _{IN} = 1.07 V	-25		
I _{I(OD)}	Minimum Bushold Over-Drive Current Needed to Change State	V _{CC} = 3.6 V, (Note 3)	450		μA
		V _{CC} = 3.6 V, (Note 4)	-450		
		V _{CC} = 2.7 V, (Note 3)	300		
		V _{CC} = 2.7 V, (Note 4)	-300		
		V _{CC} = 1.95 V, (Note 3)	200		
		V _{CC} = 1.95 V, (Note 4)	-200		
I _{OZ}	3-State Output Current	1.65 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _O ≤ 3.6 V; V _I = V _{IH} or V _{IL}		±10	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0 V; V _I or V _O = 3.6 V		10	μA
I _{CC}	Quiescent Supply Current (Note 5)	1.65 V ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		20	μA
		1.65 V ≤ V _{CC} ≤ 3.6 V; 3.6 V ≤ V _I , V _O ≤ 3.6 V		±20	
ΔI _{CC}	Increase in I _{CC} per Input	2.7 V < V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		750	μA

2. These values of V_I are used to test DC electrical characteristics only.
3. An external driver must source at least the specified current to switch from LOW-to-HIGH.
4. An external driver must source at least the specified current to switch from HIGH-to-LOW.
5. Outputs disabled or 3-state only.

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AC CHARACTERISTICS (Note 6; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500$ Ω)

Symbol	Parameter	Waveform	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						Unit
			$V_{CC} = 3.0$ V to 3.6 V		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} = 1.65$ V to 1.95 V		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input-to-Output	1	0.8 0.8	2.5 2.5	1.0 1.0	3.0 3.0	1.5 1.5	6.0 6.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	4.1 4.1	1.5 1.5	8.2 8.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	3.8 3.8	1.5 1.5	7.8 7.8	ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 7)			0.5 0.5		0.5 0.5		0.75 0.75	ns

6. For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.
 7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC CHARACTERISTICS ($t_R = t_F = 2.0$ ns; $C_L = 50$ pF; $R_L = 500$ Ω)

Symbol	Parameter	Waveform	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				Unit
			$V_{CC} = 3.0$ V to 3.6 V		$V_{CC} = 2.7$ V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input-to-Output	3	1.0 1.0	3.9 3.9		5.3 5.3	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	4	1.0 1.0	5.0 5.0		6.1 6.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	4	1.0 1.0	4.4 4.4		4.8 4.8	ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 8)			0.5 0.5		0.5 0.5	ns

8. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$	
			Typ	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 9)	$V_{CC} = 1.8\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	0.25	V
		$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	0.6	
		$V_{CC} = 3.3\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	0.8	
V _{OLV}	Dynamic LOW Valley Voltage (Note 9)	$V_{CC} = 1.8\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	-0.25	V
		$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	-0.6	
		$V_{CC} = 3.3\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	-0.8	
V _{OHV}	Dynamic HIGH Valley Voltage (Note 10)	$V_{CC} = 1.8\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	1.5	V
		$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	1.9	
		$V_{CC} = 3.3\text{ V}, C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{ V}$	2.2	

9. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

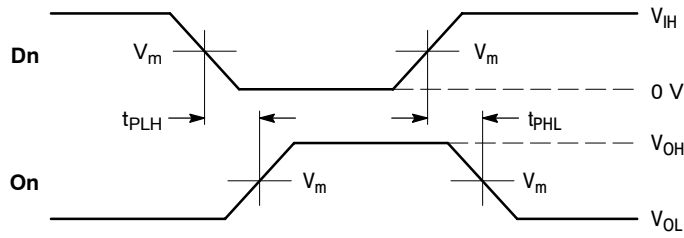
10. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	Note 11	6	pF
C _{OUT}	Output Capacitance	Note 11	7	pF
C _{PD}	Power Dissipation Capacitance	Note 11, 10 MHz	20	pF

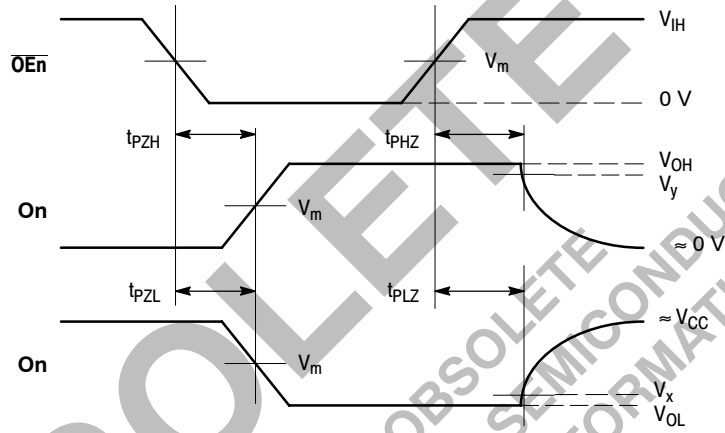
11. $V_{CC} = 1.8\text{ V}, 2.5\text{ V}$ or 3.3 V ; $V_I = 0\text{ V}$ or V_{CC} .

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WAVEFORM 1 - PROPAGATION DELAYS

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Figure 4. AC Waveforms

Table 2. AC WAVEFORMS

Symbol	V_{CC}		
	$3.3 \text{ V} \pm 0.3 \text{ V}$	$2.5 \text{ V} \pm 0.2 \text{ V}$	$1.8 \text{ V} \pm 0.15 \text{ V}$
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_m	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

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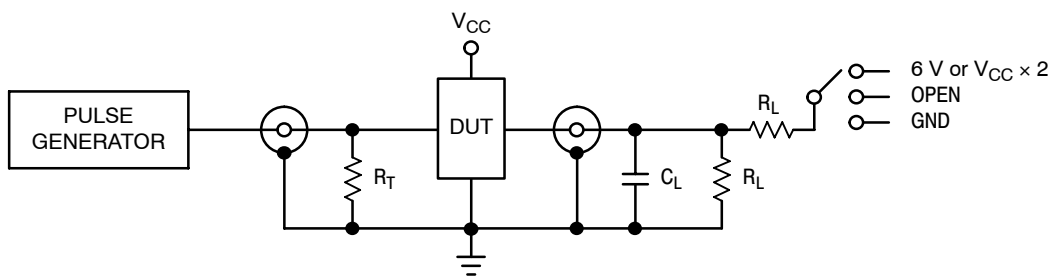


Figure 5. Test Circuit

Table 3. TEST CIRCUIT

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3$ V; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2$ V; 1.8 ± 0.15 V
t_{PZH} , t_{PHZ}	GND

$C_L = 30$ pF or equivalent (Includes jig and probe capacitance)

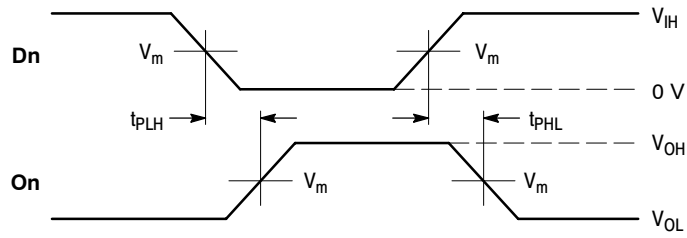
$R_L = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

OBSOLETE

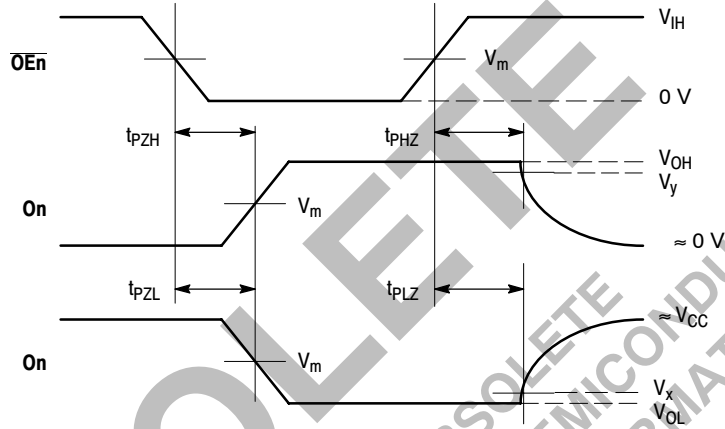
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WAVEFORM 3 - PROPAGATION DELAYS

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 4 - OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Figure 6. AC Waveforms

Table 4. AC WAVEFORMS

Symbol	V _{CC}	
	3.3 V ± 0.3 V	2.7 V
V _{IH}	2.7 V	2.7 V
V _m	1.5 V	1.5 V
V _x	V _{OL} + 0.3 V	V _{OL} + 0.3 V
V _y	V _{OH} - 0.3 V	V _{OH} - 0.3 V

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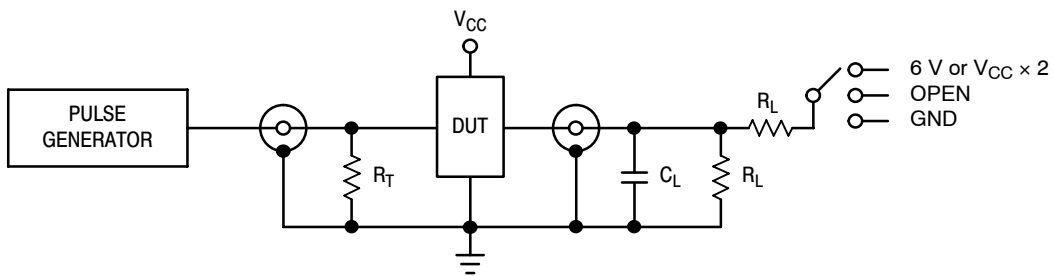


Figure 7. Test Circuit

Table 5. TEST CIRCUIT

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3$ V; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2$ V; 1.8 ± 0.15 V
t_{PZH} , t_{PHZ}	GND

$C_L = 50$ pF or equivalent (Includes jig and probe capacitance)

$R_L = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

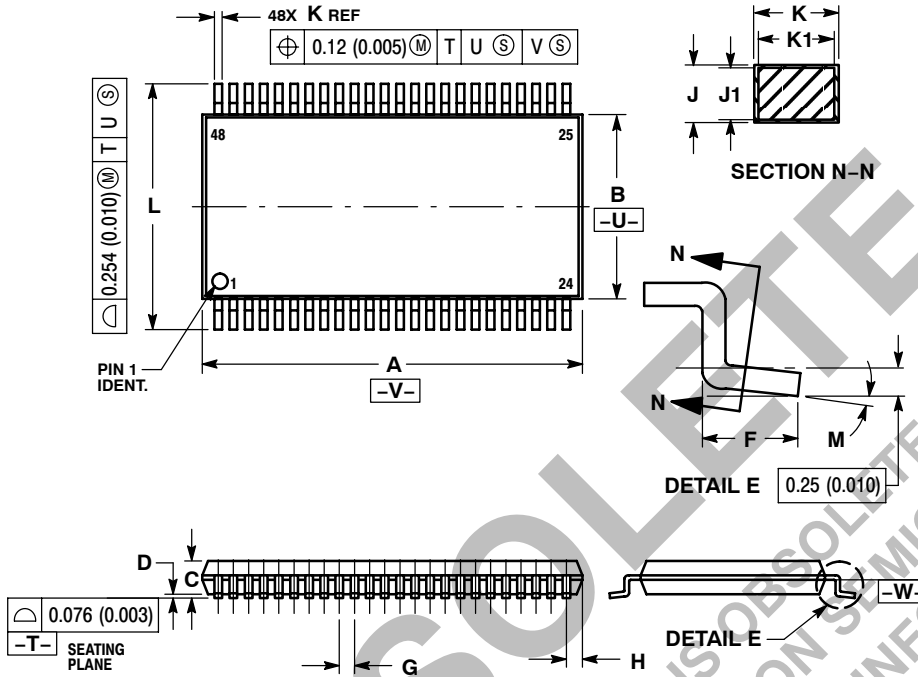
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74VCXH16240

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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